JOB 6804



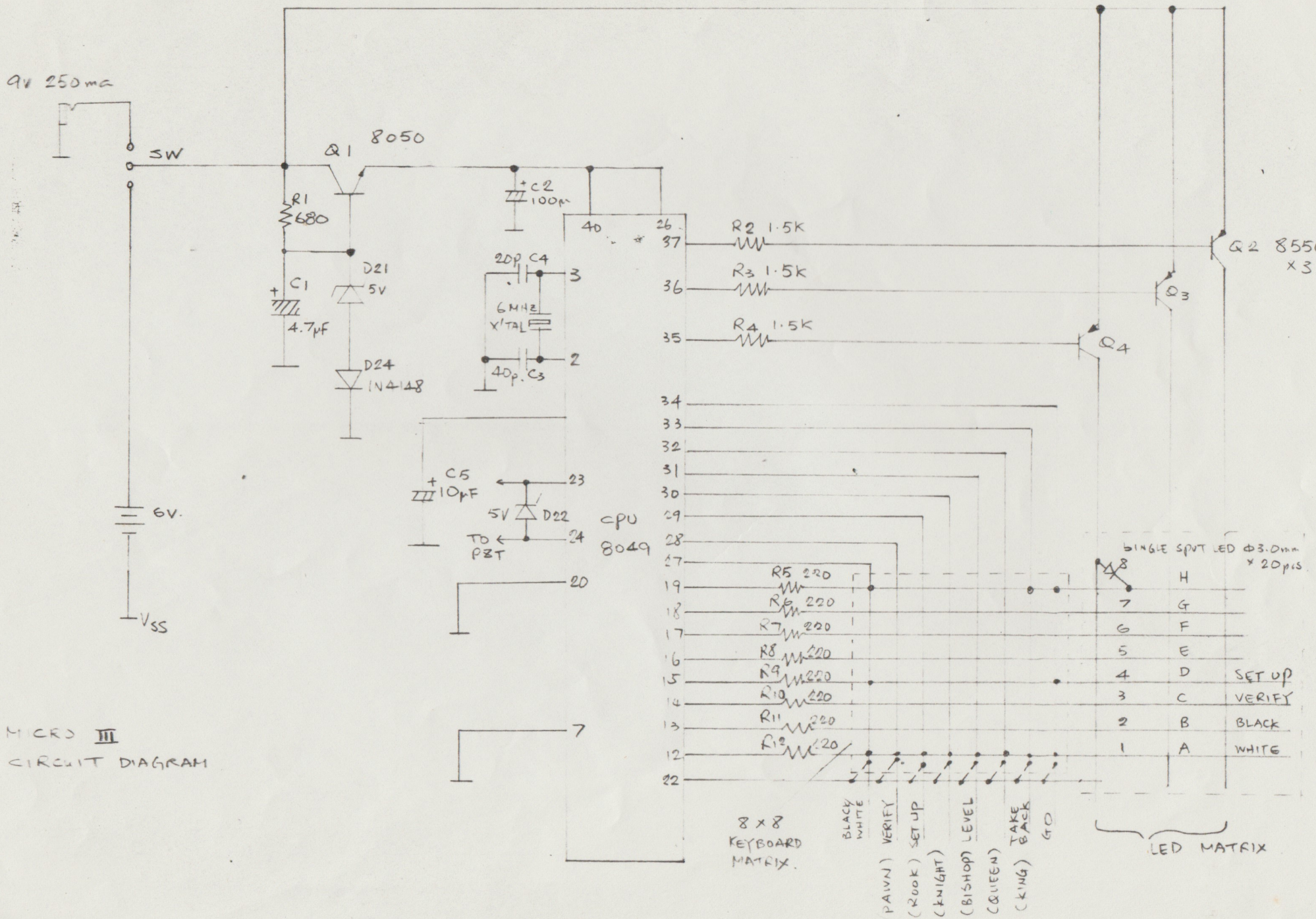


NOVAG INDUSTRIES LIMITED

# MICRO III (Art No. 841)

## SERVICE MANUAL

## CONTENTS




MICRO III
CIRCUIT DIAGRAM

MICRO III

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| ITEM | NVG P/N | DESCRIPTION | QTY | UNIT PRC (US$) |
|---|---|---|---|---|
| 13 | | JUMPER WIRE 80mm (YELLOW) | 1 | 0.01 |
| 14 | | JUMPER WIRE 90mm (BLACK) | 1 | 0.01 |
| 15 | | JUMPER WIRE 110mm (WHITE) | 2 | 0.01 |
| 16 | | JUMPER WIRE 140mm (BLACK) | 1 | 0.01 |
| 17 | | JUMPER WIRE 175mm (RED) | 1 | 0.01 |
| 18 | | BATTERY PAPER CARD | 1 | 0.04 |
| 19 | | BATTERY STRIP | 1 | 0.02 |
| 20 | | WOODGRAIN SHEET - LEFT | 1 | 0.05 |
| 21 | | WOODGRAIN SHEET - RIGHT | 1 | 0.05 |
| 22 | | WOODGRAIN SHEET - FRONT | 1 | 0.05 |

C) ASSEMBLY : PACKING

| ITEM | NVG P/N | DESCRIPTION | QTY | UNIT PRC (US$) |
|---|---|---|---|---|
| 1 | 600119 | CHESS PIECES - WHITE | 20 | 0.20/set |
| 2 | 600121 | CHESS PIECES - BLACK | 20 | 0.20/set |
| 3 | 600122 | CLEAR COVER | 1 | 0.50 |
| 4 | 970079 | INSTRUCTION MANUAL - ENGLISH | 1 | ] |
| 5 | 970080 | INSTRUCTION MANUAL - GERMAN | 1 | ] 0.30 |
| 6 | 970081 | INSTRUCTION MANUAL - FRENCH | 1 | ] |
| 7 | 990066 | GIFT BOX | 1 | 0.50 |
| 8 | | WARRANTY CARD | 1 | 0.10 |
| 9 | | POLY BAG 7"x10" | 1 | 0.04 |
| 10 | | BUBBLE BAG | 1 | 0.15 |
| 11 | | RATING LABEL - SERIAL NO | 1 | 0.08 |
| 12 | | CARTON EXPORT | 1/20 | 1.50 |
| 13 | | CARTON INNER | 1/10 | 0.50 |

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MICRO III



| ITEM | NVG P/N | DESCRIPTION | QTY | UNIT PRC (US$) |
|---|---|---|---|---|
| 23 | | ELECT CAP 100MFD | 1 | 0.05 |
| 24 | | BARE WIRE 10mm | 8 | 0.01 |
| 25 | | BARE WIRE 15mm | 6 | 0.01 |
| 26 | | JUMPER WIRE 30mm | 2 | 0.01 |
| 27 | | FOAM 10x40mm | 1 | 0.04 |
| 28 | | SCREW 2.6x12 (BLACK) | 4 | 0.01 |
| 29 | | SCREW 2x5 (BLACK) | 2 | 0.01 |
| 30 | | SCREW 2x5 (SLIVER) | 2 | 0.01 |

B) ASSEMBLY : HOUSING

| ITEM | NVG P/N | DESCRIPTION | QTY | UNIT PRC (US$) |
|---|---|---|---|---|
| 1 | 200001 | 27mm PIEZO TRANSDUCER | 1 | 0.20 |
| 2 | 350007 | JACK 5.5x2mm | 1 | 0.15 |
| 3 | 510003 | 8 KEY CONDUCTIVE RUBBER | 1 | 0.15 |
| 4 | 510017 | RUBBER FEET | 4 | 0.01 |
| 5 | 510018 | BATTERY FOAM PAD | 1 | 0.04 |
| 6 | 530050 | BATTERY CONTACT (+) | 2 | 0.05 |
| 7 | 530051 | BATTERY CONTACT (-) | 2 | 0.05 |
| 8 | 600022 | BATTERY DOOR | 1 | 0.05 |
| 9 | 600116 | TOP HOUSING | 1 | 0.80 |
| 10 | 600117 | BOTTOM HOUSING | 1 | 0.30 |
| 11 | 600118 | KEYTOPS | 8 | 0.08/set |
| 12 | 600120 | KEYBOARD FRAME | 1 | 0.15 |

cont'd /3

BILL OF MATERIALS

MODEL : MICRO III (841)

A) ASSEMBLY : MAIN PCB

| ITEM | NVG P/N | DESCRIPTION | QTY | UNIT PRC (US$) |
|---|---|---|---|---|
| 1 | 010011 | CPU 80C49 | 1 | 6.60 |
| 2 | 050008 | LED 3mm - RED | 16 | 0.10 |
| 3 | 050009 | LED 3mm - GREEN | 4 | 0.10 |
| 4 | 100012 | KEYBOARD PCB | 1 | 0.15 |
| 5 | 100013 | LOGIC PCB | 1 | 0.45 |
| 6 | 110003 | 8x8 CHOMERIC KEYBOARD | 1 | 0.80 |
| 7 | 130007 | 1P2T SLIDE SWITCH | 1 | 0.10 |
| 8 | 400017 | 8 PIN CONNECTOR RIGHT ANGLE | 2 | 0.40 |
| 9 | 410018 | 9 PIN CONNECTOR ARRAY | 1 | 0.15 |
| 10 | 510015 | RUBBER SHEET | 1 | 0.10 |
| 11 | | O.S.C. COIL 40 UH | 1 | 0.10 |
| 12 | | RESISTOR 330 OHM | 8 | 0.01 |
| 13 | | RESISTOR 1.2K OHM | 1 | 0.01 |
| 14 | | RESISTOR 1.5K OHM | 3 | 0.01 |
| 15 | | TR8050/9013H | 1 | 0.10 |
| 16 | | TR 8550/9012H | 3 | 0.10 |
| 17 | | ZENER DIODE 5.6V | 2 | 0.10 |
| 18 | | DIODE IN4148 | 1 | 0.05 |
| 19 | | CERAMIC CAP 39PF | 1 | 0.01 |
| 20 | | CERAMIC CAP 47PF | 1 | 0.01 |
| 21 | | ELECT CAP 1 MFD | 1 | 0.05 |
| 22 | | ELECT CAP 10 MFD | 1 | 0.05 |

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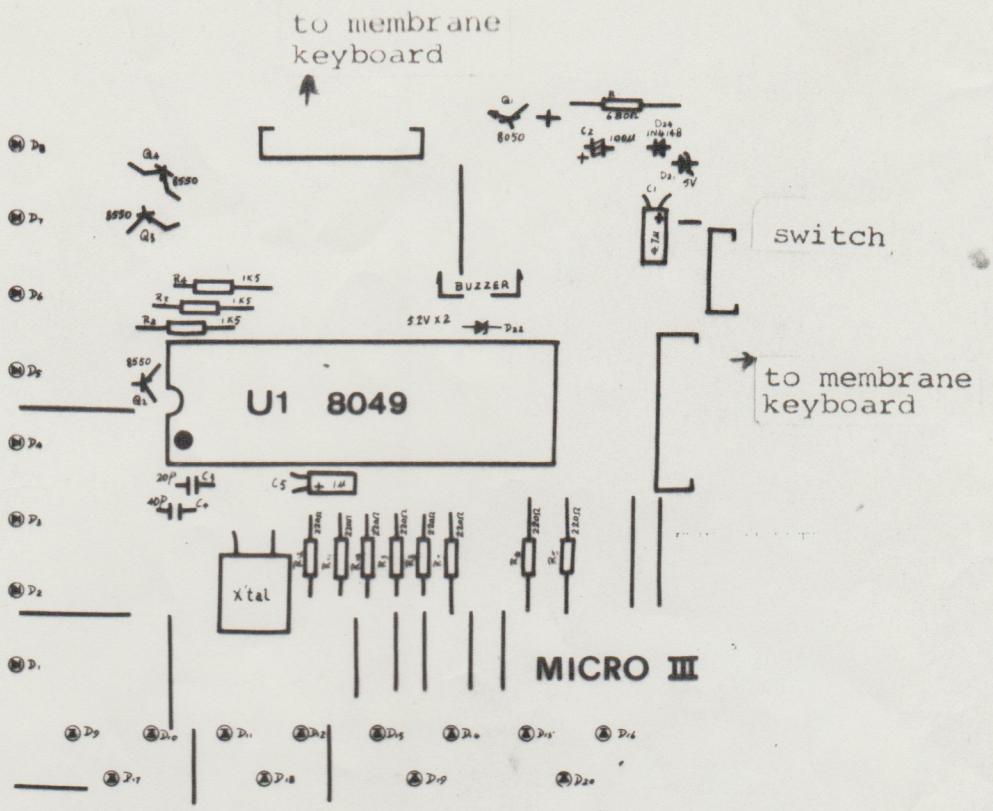
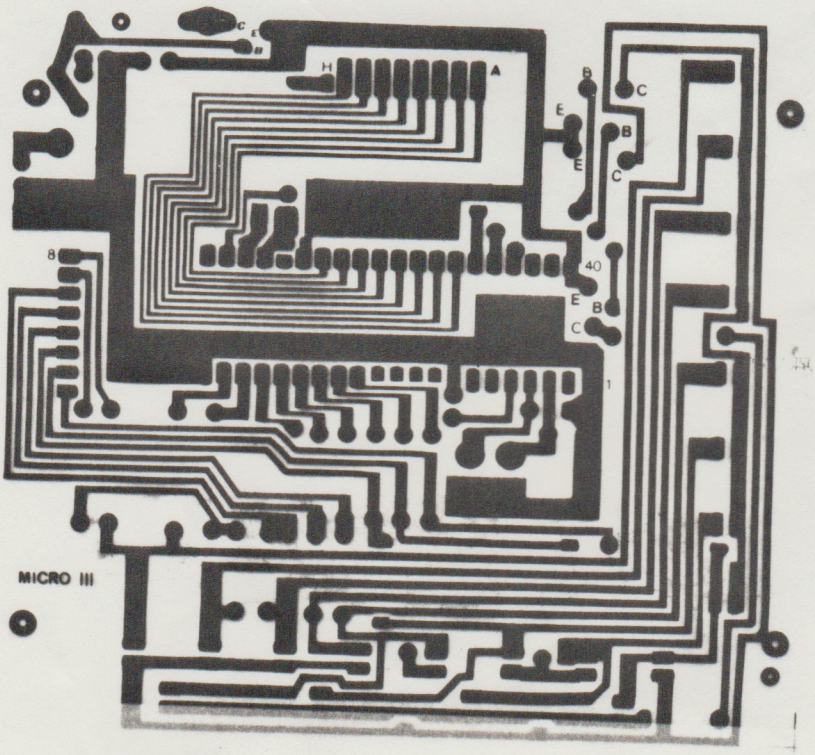
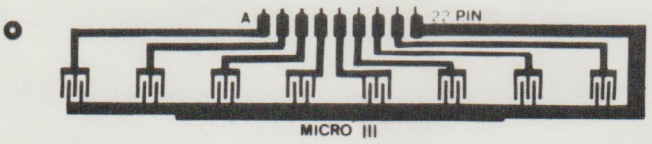



MICRO III Logic PCB Layout w/components location






MICRO III KEYBOARD PCB LAYOUT

# M5L8049-XXXP,P-8,P-6
# M5L8039P-11,P-8,P-6

## SINGLE-CHIP 8-BIT MICROCOMPUTER

## DESCRIPTION

The M5L8049-XXXP, P-8, P-6 and M5L8039P-11, P-8, P-6 are 8-bit parallel microcomputers fabricated on a single chip using high-speed N-channel silicon gate ED-MOS technology.

| Speed \ ROM Type | Internal ROM Type | External ROM Type |
|---|---|---|
| 11 MHz Type | M5L8049-XXXP | M5L8039P-11 |
| 8 MHz Type | M5L8049-XXXP-8 | M5L8039P-8 |
| 6 MHz Type | M5L8049-XXXP-6 | M5L8039P-6 |

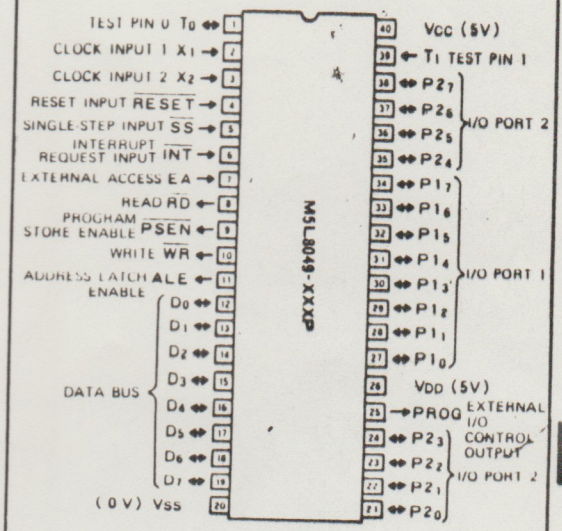
## FEATURES

- Single 5V power supply
- Basic machine instructions . . . . . 96
  - 1-byte instructions: 68
  - 2-byte instructions: 28
- Direct addressing . . . . . up to 4096 bytes
- Internal RAM . . . . . 128 bytes
- Built-in timer/event counter . . . . . 8 bits
- I/O Ports . . . . . 27 lines
- Easily expandable Memory and I/O:
- Subroutine nesting . . . . . 8 levels
- External and timer/event counter interrupt . 1 level each
- External RAM . . . . . 256 bytes
- M5L8049-XXXP/M5L8039P-11, P-6 are interchangeable with Intel's P8049/P8039, P8039-6 in pin configuration and electrical characteristics.

## APPLICATION

- Control processor or CPU for a wide variety of applications

## PIN CONFIGURATION (TOP VIEW)

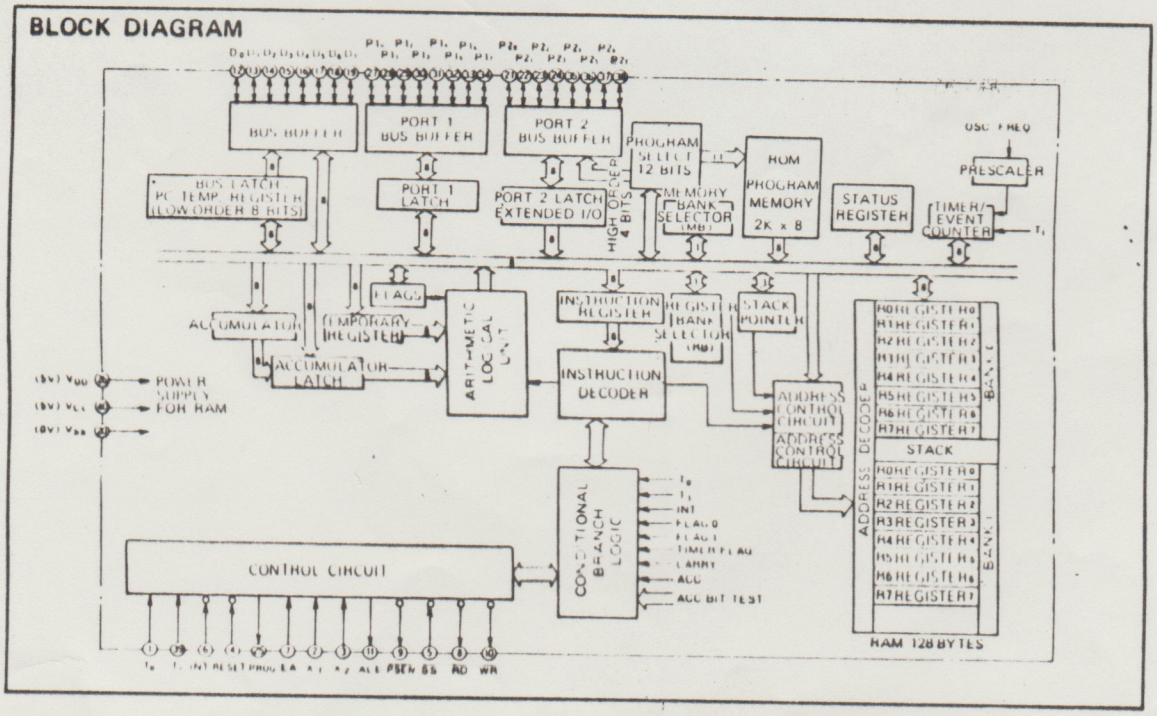



Outline 40P1

## FUNCTION

The M5L8049-XXXP and M5L8039P are integrated 8-bit CPUs, with memory (ROM, RAM) and timer/event counter interrupt all contained on a single chip.

## BLOCK DIAGRAM



# M5L8049-XXXP,P-8,P-6
# M5L8039P-11,P-8,P-6

## SINGLE-CHIP 8-BIT MICROCOMPUTER

## PIN DESCRIPTION

| Pin | Name | Input or Output | Function |
|---|---|---|---|
| $V_{SS}$ | Ground | | Normally connected to ground (0V) |
| $V_{CC}$ | Main power supply | | Connected to 5V power supply |
| $V_{DD}$ | Power supply | | ① Connected to 5V power supply<br>② Used for memory hold when $V_{CC}$ is cut |
| PROG | Program | Output | Strobe signal for M5L8243P I/O Expander |
| $P1_0$ ~ $P1_7$ | Port 1 | Input/output | Quasi bidirectional port. When used as an input port, $FF_{16}$ must first be output to this port. After reset, when not used as an output port nothing can be output. |
| $P2_0$ ~ $P2_3$ | Port 2 | Input/output | ① The same as port 1 |
| | | Output | ② $P2_0$~$P2_3$ output the high order 4 bits of the program counter when using external program memory |
| | | Input/output | ③ $P2_0$~$P2_3$ serve as a 4-bit I/O expander bus for the M5L8243P |
| $D_0$ ~ $D_7$ | Data bus | Input/output | ① Provides true bidirectional bus transfer of instructions and data between the CPU and external memory. Synchronizing is done with signals $\overline{RD}$/$\overline{WR}$. The output data is latched.<br>② When using external program memory the output of the low-order 8 bits of the program counter are synchronized with ALE. After that the transfer of the instruction code or data from external program memory is synchronized with $\overline{PSEN}$.<br>③ The output of addresses for data using extern l data memory is synchronized with ALE. After that the transfer of data with the external data memory is synchronized with RD/WR<br>(MOVX A, @Rr and MOVX @Rr, A) |
| $T_0$ | Test pin 0 | Input | ① Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions.<br>(JT0 m and JNT0 m) |
| | | Output | ② Used for outputting the internal clock signal. (ENT0 CLK) |
| $T_1$ | Test pin 1 | Input | ① Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions. (JT1 m and JNT1 m)<br>② When enabled event signals are transferred to the timer/event counter. (STRT CNT) |
| $\overline{INT}$ | Interrupt | Input | ① Control signal from an external source for conditional jumping in a program. Jumping is dependent on external conditions. (JNI m)<br>② Used for external interrupt to CPU |
| $\overline{RD}$ | Read control | Output | Read control signal used when the CPU requests data from external data memory or external devices to be transferred to the data bus.<br>(MOVX A, @Rr and INS A, BUS) |
| $\overline{WR}$ | Write control | Output | Write control signal used when the CPU sends data through the data bus to external data memory or external device.<br>(MOVX @R, A and OUTL BUS, A) |
| $\overline{RESET}$ | Reset | Input | Control used to initialize the CPU |
| ALE | Address latch enable | Output | A signal used for latching the address on the data bus. An ALE signal occurs once during each cycle. |
| $\overline{PSEN}$ | Program store enable | Output | Strobe signal to fetch external program memory. |
| $\overline{SS}$ | Single step | Input | Control signal used in conjunction with ALE to stop the CPU through each instruction, in the single step mode. |
| EA | External access | Input | ① Normally maintained at 0V.<br>② When the level is raised to 5V, external memory will be accessed even when the address is less than $400_{16}$ (2048) |
| $X_1$, $X_2$ | Crystal inputs | Input | External crystal oscillator or RC circuit input for generating internal clock signals. An external clock signal can be input through $X_1$ or $X_2$. |

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Limits | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$ | −0.5 ~ 7 | V |
| $V_{DD}$ | Supply voltage | | −0.5 ~ 7 | V |
| $V_I$ | Input voltage | | −0.5 ~ 7 | V |
| $V_O$ | Output voltage | | −0.5 ~ 7 | V |
| Pd | Power dissipation | Ta = 25℃ | 1.5 | W |
| Topr | Operating free-air temperature range | | 0 ~ 70 | ℃ |
| Tstg | Storage temperature range | | −65 ~ 150 | ℃ |

## RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70℃, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{DD}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{SS}$ | Supply voltage | | 0 | | V |
| $V_{IH1}$ | High-level input voltage, except for $X_1$, $X_2$, RESET | 2 | | $V_{CC}$ | V |
| $V_{IH2}$ | High-level input voltage, $X_1$, $X_2$, RESET | 3.8 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage | 0.5 | | 0.8 | V |

## ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 70℃, $V_{CC}$ = $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{OL}$ | Low-level output voltage, BUS, RD, WR, PSEN, ALE | $I_{OL}$ = 2mA | | | 0.45 | V |
| $V_{OL1}$ | Low-level output voltage, except for the above and PROG | $I_{OL}$ = 1.6mA | | | 0.45 | V |
| $V_{OL2}$ | Low-level output voltage PROG | $I_{OL}$ = 1mA | | | 0.45 | V |
| $V_{OH}$ | High-level output voltage, BUS, RD, WR, PSEN, ALE | $I_{OH}$ = −100μA | 2.4 | | | V |
| $V_{OH1}$ | High-level output voltage, except for the above | $I_{OH}$ = −50μA | 2.4 | | | V |
| $I_{IL}$ | Input leak current, T1, INT | $V_{SS} \leq V_{IN} \leq V_{CC}$ | −10 | | 10 | μA |
| $I_{OL}$ | Output leak current, BUS, TO, high-impedance state | $V_{SS}+0.45 \leq V_{IN} \leq V_{CC}$ | −10 | | 10 | μA |
| $I_{LI1}$ | Input current during low-level input, port | $V_{IL}$ = 0.8V | | −0.2 | | mA |
| $I_{LI2}$ | Input current during low level input, RESET, SS | $V_{IL}$ = 0.8V | | 0.05 | | mA |
| $I_{DD}$ | Supply current from $V_{DD}$ | Ta = 25℃ | | 25 | 50 | mA |
| $I_{DD}+I_{CC}$ | Supply current from $V_{DD}$ and $V_{CC}$ | Ta = 25℃ | | 100 | 170 | mA |

## TIMING REQUIREMENTS (Ta = 0 ~ 70℃, $V_{CC}$ = $V_{DD}$ = 5V ± 10%, $V_{SS}$ = 0V, unless otherwise noted)

| Symbol | Parameter | Alternative symbol | Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | M5L8049-XXXP M5L8039P-11 | | | M5L8049-XXXP-8 M5L8039P-8 | | | M5L8049-XXXP-6 M5L8039P-6 | | | |
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| tc | Cycle time | $t_{CY}$ | 1.36 | | 15.0 | 1.875 | | 15.0 | 2.5 | | 15.0 | μs |
| th (PSEN-D) | Data hold time after PSEN | $t_{DR}$ | 0 | | 100 | 0 | | 150 | 0 | | 200 | ns |
| th (R-D) | Data hold time after RD | $t_{DR}$ | 0 | | 100 | 0 | | 150 | 0 | | 200 | ns |
| tsu (PSEN-D) | Data setup time after PSEN | $t_{RD}$ | | | 250 | | | 350 | | | 500 | ns |
| tsu (R-D) | Data setup time after RD | $t_{RD}$ | | | 250 | | | 350 | | | 500 | ns |
| tsu (A-D) | Data setup time after address | $t_{AD}$ | | | 400 | | | 650 | | | 950 | ns |
| tsu (PROG-D) | Data setup time after PROG | $t_{PR}$ | | | 650 | | | 700 | | | 810 | ns |
| th (PROG-D) | Data hold time before PROG | $t_{PF}$ | 0 | | 150 | 0 | | 150 | 0 | | 150 | ns |

Note 1 The input voltages are $V_{IL}$ = 0.45V and $V_{IH}$ = 2.4V

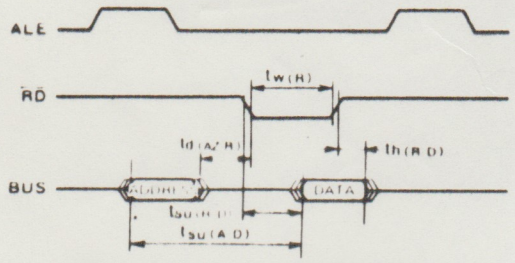
## SWITCHING CHARACTERISTICS ($T_a$ = 0~70°C, $V_{CC}$ = $V_{DD}$ = 5V±10%, $V_{SS}$ = 0V, unless otherwise noted)

| Symbol | Parameter | Alternative symbol | Limits | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | M5L8049P-XXXP, M5L8039P-11 | | | M5L8049P-XXXP-8, M5L8039P-8 | | | M5L8049-XXXP-6, M5L8039P-6 | | | |
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{W(ALE)}$ | ALE pulse width | $t_{LL}$ | 150 | | | 300 | | | 400 | | | ns |
| $t_{d(A-ALE)}$ | Delay time, address to ALE signal | $t_{AL}$ | 70 | | | 120 | | | 150 | | | ns |
| $t_{v(ALE-A)}$ | Address valid time after ALE | $t_{LA}$ | 50 | | | 70 | | | 80 | | | ns |
| $t_{W(PSEN)}$ | PSEN pulse width | $t_{CC}$ | 300 | | | 500 | | | 700 | | | ns |
| $t_{W(R)}$ | $\overline{RD}$ pulse width | $t_{CC}$ | 300 | | | 500 | | | 700 | | | ns |
| $t_{d(W)}$ | $\overline{WR}$ pulse width | $t_{CC}$ | 300 | | | 500 | | | 700 | | | ns |
| $t_{v(Q-W)}$ | Delay time, data to $\overline{WR}$ signal | $t_{DW}$ | 250 | | | 380 | | | 500 | | | ns |
| $t_{d(W-Q)}$ | Data valid time after $\overline{WR}$ | $t_{WD}$ | 40 | | | 80 | | | 120 | | | ns |
| $t_{d(A-W)}$ | Delay time, address to $\overline{WR}$ signal | $t_{AW}$ | 200 | | | 220 | | | 230 | | | ns |
| $t_{d(AZ-R)}$ | Delay time, address disable to $\overline{RD}$ signal | $t_{AFC}$ | 10 | | | 5 | | | 0 | | | ns |
| $t_{d(AZ-PSEN)}$ | Delay time, address disable to $\overline{PSEN}$ signal | $t_{AFC}$ | −10 | | | 5 | | | 0 | | | ns |
| $t_{d(PC-PROG)}$ | Delay time, port control to $\overline{PROG}$ signal | $t_{CP}$ | 100 | | | 105 | | | 110 | | | ns |
| $t_{v(PROG-PC)}$ | Port control valid time after $\overline{PROG}$ | $t_{PC}$ | 60 | | | 100 | | | 130 | | | ns |
| $t_{p(Q-PROG)}$ | Delay time, data to $\overline{PROG}$ signal | $t_{DP}$ | 200 | | | 210 | | | 220 | | | ns |
| $t_{v(PROG-Q)}$ | Data valid time after $\overline{PROG}$ | $t_{PD}$ | 20 | | | 45 | | | 65 | | | ns |
| $t_{W(PROGL)}$ | $\overline{PROG}$ low pulse width | $t_{PP}$ | 700 | | | 1150 | | | 1510 | | | ns |
| $t_{d(Q-ALE)}$ | Delay time, data to ALE signal | $t_{PL}$ | 150 | | | 300 | | | 400 | | | ns |
| $t_{v(ALE-Q)}$ | Data valid time after ALE | $t_{LP}$ | 20 | | | 100 | | | 150 | | | ns |

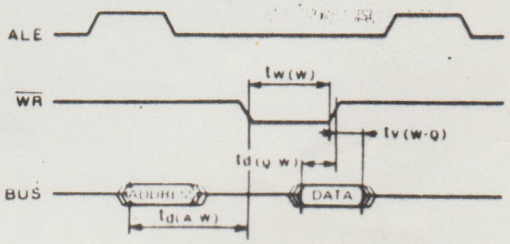
Note 2 Conditions of measurement: control output $C_L$ = 80pF
data bus output, port output $C_L$ = 150pF, $t_r$, $t_f$ = 20ns (Max)
1 Reference level for the input output waveform: low level 0.8V and high level 2V

## TIMING DIAGRAM

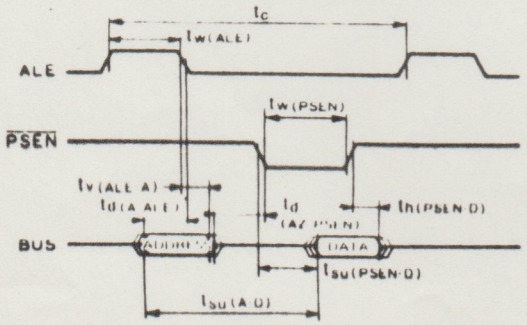
### Read from External Data Memory



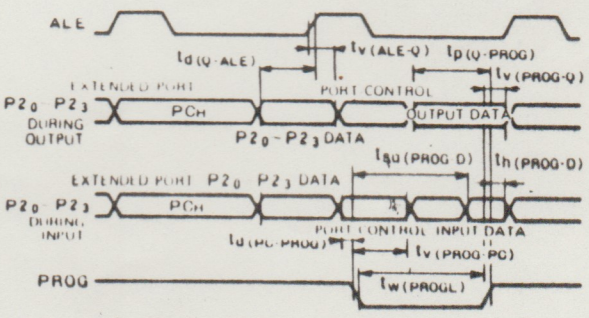

### Write to External Data Memory




### Instruction Fetch from External Program Memory




### Port 2






MITSUBISHI ELECTRIC